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34705	7590	08/09/2006	EXAMINER	
			MOORE, IAN N	
			ART UNIT	PAPER NUMBER
			2616	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/883,075	DONIS ET AL.	
Examiner	Art Unit		
Ian N. Moore	2616		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### **Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 14 July 2006.

2a)  This action is **FINAL**.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 1,2,4-9,11-17 and 33-43 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1,2,4-9,11-17,33-43 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_

4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_\_

## DETAILED ACTION

### First set of rejection

#### *Claim Rejections - 35 USC § 102 (e)*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 4-9, 11-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Fan (US 6,324,165), as set forth in **previous** office action, and hereby incorporated. Examiner also asserts the buffer capacity as “buffer/queue capacity” as set forth in previous office action.

### Second set of rejection

3. Claims 1,2,6-9,11-17,33-37,42 and 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Caldara (US005872769A).

**Regarding Claims 1 and 9**, Caldara discloses a switch (see FIG. 1 and 6; ATM switch) for a communication network (see col. 1, line 16-35; in a ATM network), the switch comprising: a plurality of ports (see FIG. 1, Input ports 0-n 20 and Output port 0-n 22); a first buffer memory (see FIG. 1-2, first Input/output queue 32/34, FIG. 6, Pri#1 or VBR buffer/queue) having a first queue capacity (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold/capacity of first

Input/output buffer/queue) coupled to one of the ports (see FIG. 1, couple to input/output ports) to store communication units (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells) corresponding to a first quality of service level (see FIG. 6, storing in Pri#1 or VBR; see col. 8, line 65 to col. 9, line 40);

a second buffer memory (see FIG. 1-2, second Input/output queue 32/34; FIG. 6, Pri#4 or ABR buffer/queue) having a second queue capacity (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold/capacity of second Input/output buffer/queue) coupled to the one of the ports (see FIG. 1, couple to input/output ports) to store communication units corresponding to a second quality of service level (see FIG. 6, storing in Pri#4 or ABR; see col. 8, line 65 to col. 9, line 40); and

a buffer manager (see FIG. 1, a combined system of control in To/From Switch Port Processor 14/16 and Bandwidth Arbiter (BA) 12; see col. 4, line 32-64), coupled to the first buffer memory and the second buffer memory (see FIG. 1, a combined bandwidth control and Arbiter system couples to first and second priority queues/buffers), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication units, and to retrieve communication units from the first buffer memory and the second buffer memory (see FIG. 1, 6, a combined bandwidth and control system stores/writes/input and retrieves/read/output the cells to/from first and second priority queues/buffers; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67), and to adjust a capacity of at least one of the first queue capacity of the first buffer memory or the second queue capacity of the second buffer memory (see col. 7, line 30-65; see col. 8, line 19 to

col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined system of bandwidth control and arbiter dynamically manages/adjusts each queue for dynamic threshold/capacity).

**Regarding Claim 2**, Caldara discloses a sorter unit (see FIG. 1, a combined scheduling/sorting system of Switch Allocation Table (SAT) (see FIG. 3) and BA 12) coupled to the first buffer memory and the second buffer memory to selectively store a communication unit in the first buffer or the second buffer based on a quality of service level of the communication unit (see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67; the combined switching system schedules/sorts the ATM cells according to their service classes).

**Regarding Claim 6**, Caldara discloses means for determining performance characteristics of the buffer element (see FIG. 1, a combined system of control in To/From Switch Port Processor 14/16 and Bandwidth Arbiter (BA) 12 determines performance of the switch 10; see col. 4, line 32-64).

**Regarding Claim 7**, Caldara discloses the first buffer memory and the second buffer memory are regions of memory in a contiguous random access memory device (see col. 5, line 65 to col. 6, line 4; each TSPP/ includes cell buffer RAM which are organized/contiguous into queues).

**Regarding Claims 8, 17 and 42**, Caldara discloses wherein the communication units are ATM cells (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells).

**Regarding Claim 11**, Caldara discloses a plurality of output ports (see FIG. 1, Output port 0-n) that output communication units from the switch to the network (see col. 5, line 35-50; output ports connects the switch 10 to ATM network); and

the first buffer memory and the second buffer memory (see FIG. 1-2, first and second Input queue 32 a-m) are coupled to one of the plurality of output ports (see FIG. 1, Output port 0-n), to store communication units to be output to the one of the plurality of output ports (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; Input queues stores ATM cells to output to output ports).

**Regarding Claim 12**, Caldara discloses each of the plurality of output ports has a respective first buffer memory (see FIG. 1-2, first output queue 34 a) and a respective second buffer memory (see FIG. 1-2, second output queue 34 m) to store communication units transmitted across the respective output port (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; first and second output queues stores ATM cells which are transmitted to output port).

**Regarding Claim 13**, Caldara discloses each of the plurality of output ports has a respective buffer manager (see FIG. 1, a control in output port) to selectively store communication units in the respective first buffer and the respective second buffer (see FIG. 1-2, first and second output queue 34 a and m) based on a corresponding quality of service level of the communication units (see FIG. 6, storing in VBR or ABR output queues; see col. 8, line 65 to col. 9, line 40), and to retrieve communication units from the respective first buffer memory and the respective second buffer memory (see FIG. 1, 6, control processor in the stores/writes/input and retrieves/read/output the cells to/from first and second output queues; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67).

**Regarding Claim 14**, Caldara discloses a plurality of input ports (see FIG. 1, Input ports 0-n 20) that receive communication units from the switch to the network (see col. 5, line 35-50;

input ports receives ATM cells the switch 10 to ATM network); and the first buffer memory (see FIG. 1-2, first output queue 34 a) and the second buffer memory (see FIG. 1-2, first output queue 34 m) are coupled to one of the plurality of input ports (see FIG. 1, Input ports 0-n 20), to store communication units received on the one of the plurality of input ports (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; Output queues 34 stores ATM cells receives from input ports).

**Regarding Claim 15**, Caldara discloses each of the plurality of input ports (see FIG. 1, Input ports 0-n 20) has a respective first buffer memory (see FIG. 1-2, first Input queue 32 a) and a respective second buffer memory (see FIG. 1-2, second Input queue 32 m) to store communication units transmitted across the respective input port (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; first and second input queues stores ATM cells which are transmitted across input port).

**Regarding Claim 16**, Caldara discloses each of the plurality of input ports has a respective buffer manager (see FIG. 1, a control in input port) to selectively store communication units in the respective first buffer and the respective second buffer (see FIG. 1-2, first and second input queue 32 a and m) based on a corresponding quality of service level of the communication unit, and to retrieve communication units from the respective first buffer memory and the respective second buffer memory (see FIG. 1, 6, control processor in the stores/writes/input and retrieves/read/output the cells to/from first and second input queues; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67).

**Regarding Claims 33 and 43,** Caldara discloses a buffer element (see FIG. 1 and 6; ATM switch) for a communication network (see col. 1, line 16-35; in a ATM network), the buffer element comprising:

a first buffer memory (see FIG. 1-2, first Input/output queue 32/34, FIG. 6, Pri#1 or VBR buffer/queue) having a first capacity (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold/capacity of first Input/output buffer/queue) to store communication units (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells) corresponding to a first quality of service level (see FIG. 6, storing in Pri#1 or VBR; see col. 8, line 65 to col. 9, line 40);

a second buffer memory (see FIG. 1-2, second Input/output queue 32/34; FIG. 6, Pri#4 or ABR buffer/queue) having a second capacity (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold/capacity of second Input/output buffer/queue) to store communication units (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells) corresponding to a second quality of service level (see FIG. 6, storing in Pri#4 or ABR; see col. 8, line 65 to col. 9, line 40); and

a buffer manager (see FIG. 1, a combined system of control in To/From Switch Port Processor 14/16 and Bandwidth Arbiter (BA) 12; see col. 4, line 32-64), coupled to the first buffer memory and the second buffer memory (see FIG. 1, a combined bandwidth control and Arbiter system couples to first and second priority queues/buffers), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication units, to retrieve communication units from the first buffer memory and the second buffer memory (see FIG. 1, 6, a combined bandwidth and control system

stores/writes/input and retrieves/read/output the cells to/from first and second priority queues/buffers; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67), and to adjust at least one of the first capacity of the first buffer memory or the second capacity of the second buffer memory (see col. 7, line 30-65; see col. 8, line 19 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined system of bandwidth control and arbiter dynamically manages/adjusts each queue for dynamic threshold/capacity), based on a total memory available to the buffer element (see FIG. 7, total bandwidth available (i.e. total of used & unused bandwidth threshold), the first and second capacities (see FIG. 7, used bandwidth thresholds/capacities by the queues), and the quality of service provided by each buffer memory (see col. 9, line 1-40; service quality of each queue); see col. 7, line 30-65; see col. 8, line 52 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67.

**Regarding Claim 34**, Caldara discloses wherein the characteristic is selected from the group consisting the communication unit processing rate for one of the quality of service levels (see col. 6, line 30-40; see col. 14, line 21-27; switch utilization/processing rate for quality service classes) and the communication unit delay rate for one of the quality of service levels (see col. 1, line 27-50; see col. 2, line 64 to col. 3, line 6; see col. 7, line 40-46; see col. 9, line 21-40; see col. 13, line 33-40; delay bound/parameter/rate for service class priorities).

**Regarding Claims 35 and 36**, Caldara discloses each of the plurality of buffers (see FIG. 1-2, and 6; Input/output queues 32/34) stores communication units for a single port wherein the single port is an output port (see FIG. 1 and 6, Output port 0) in a communication network switch (see FIG. 1,2,6; ATM switch 10); see col. 4, line 50-65; col. 8, line 65 to col. 9, line 40.

**Regarding Claims 37,** Caldara discloses wherein the plurality of buffers (see FIG. 1-2, and 6; Input/output queues 32/34) stores the communication units for each port of a switch in the communication network (see FIG. 1 and 6, Input or Output port 0-n); see col. 4, line 50-65; col. 8, line 65 to col. 9, line 40.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 4,5,40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caldara in view of Holender (US006069894A).

**Regarding Claims 4 and 40,** Caldara discloses means for iteratively determining possible capacity assignments to determine the first capacity and the second capacity (see col. 7, line 30-65; see col. 8, line 52 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined system of bandwidth control and arbiter dynamically determines each queue for dynamic threshold/capacity).

Caldara does not explicitly disclose iteratively searching possible assignments. However, Holender teaches iteratively searching possible assignments to determine the optimal value in ATM network (see col. 5, line 42-46; see col. 13, line 39-60; col. 16, line 10 to col. 17, line 27; hill climbing process is used to search possible assignment/value to determine optimize threshold/value). Therefore, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to provide hill climbing search process, as taught by Holender in the system of Caldara, so that it would avoid overload situation and provide load balancing in accordance with optimization method; see Holender col. 16, line 9-16; see col. 17, line 33-37; see col. 4, line 10-64.

**Regarding Claims 5 and 41**, the combined system of Caldara and Holender discloses all limitation as described above in claim 1. Holender further teaches means for performing a steepest ascent hill-climbing search (see col. 5, line 42-46; see col. 13, line 39-60; col. 16, line 10 to col. 17, line 27; ascend or step hill climbing process is used to search possible assignment/value to determine optimize threshold/value). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide hill climbing search process, as taught by Holender in the system of Caldara, so that it would avoid overload situation and provide load balancing in accordance with optimization method; see Holender col. 16, line 9-16; see col. 17, line 33-37; see col. 4, line 10-64.

6. Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caldara in view of Kakuma (US005555265A).

**Regarding Claim 38**, Caldara discloses determining a priority level for communication units for each of the quality of service levels as described above in claim 33.

Caldara does not explicitly disclose level for dropped. However, Kakuma teaches determining a priority level for dropped communication units for each of the quality of service levels (see col. 5, line 33-67; determining discard priority for each quality class). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was

made to provide determining discard priority for each quality class, as taught by Kakuma in the system of Caldara, so that it would prevent each service from adversely affecting other service and allow the quality of service to be easily controlled; see Kakuma col. 3, line 10-15.

**Regarding Claim 39**, Caldara discloses determining a priority level for communication units for each of the quality of service levels as described above in claim 33.

Caldara does not explicitly disclose delay for quality service level. However, Kakuma teaches determining a priority level for communication units delay for each of the quality of service levels (see col. 14, line 45-65; see col. 15, line 20-34; determining delay priority for each quality class). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide determining delay priority for each quality class, as taught by Kakuma in the system of Caldara, so that it would prevent each service from adversely affecting other service and allow the quality of service to be easily controlled; see Kakuma col. 3, line 10-15.

***Claim Rejections - 35 USC § 102 (b)***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 9, 33 and 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamada (US005581544A).

**Regarding Claims 1 and 9,** Hamada discloses a switch (see FIG. 1-2; ATM multiplexing apparatus; see col. 2, line 49-50; see col. 6, line 45-55) for a communication network (see FIG. 1, ATM network; see col. 1, line 20-25), the switch comprising:

- a plurality of ports (see FIG. 1, interfaces/ports at Mux 12 that couples to different lines 10 (P0-2));
- a first buffer memory (see FIG. 2, Highest priority FIFO buffer Q0) having a first queue capacity (see col. 6, line 65 to col. 7 line 4; see col. 11, line 60-67; cell count/capacity in a buffer, or buffer amount/capacity (i.e. Q0 buffer)) coupled to one of the ports (see FIG. 2, Q0 couple to P0 port) to store communication units (see col. 6, line 55-60; storing ATM cells) corresponding to a first quality of service level (see FIG. 2, storing in priority P0 class of highest QoS; see col. 6, line 56-63; col. 11, line 59-62);
- a second buffer memory (see FIG. 2, lower priority FIFO buffer Q1 or Q2) having a second queue capacity (see col. 6, line 65 to col. 7 line 4; see col. 11, line 60-67; cell count/capacity in buffer, or buffer amount/capacity (i.e. Q1 or Q2 buffer)) coupled to the one of the ports (see FIG. 2, Q1 or Q2 couple to P0 or P1 port) to store communication units (see col. 6, line 55-60; storing ATM cells) corresponding to a second quality of service level (see FIG. 2, storing in priority P1 or P2 class of lower QoS; see col. 6, line 56-63; col. 11, line 59-62); and
- a buffer manager (see FIG. 1, a controller 14; see col. 6, line 45-50), coupled to the first buffer memory and the second buffer memory (see FIG. 1, controller 12 couples to Mux 12, which contains Q0 and Q1/2 buffers), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication units (see FIG. 2 and FIG. 3, step 1002,1004 with call admitted; see col. 6, line 52-64; see col.

11, line 55-57; QoS of each admitted cell is determined and stores in corresponding Q0, Q1 or Q2 buffer, respectively), and to retrieve communication units from the first buffer memory and the second buffer memory (see FIG. 2; see col. 6, line 52-64; each buffered cell are outputted from Q0, Q1 or Q2 buffer, respectively), and to adjust a capacity of at least one of the first queue capacity of the first buffer memory or the second queue capacity of the second buffer memory (see FIG. 4, step 1102,1104,1106,1108,1110,1112; see col. 11, line 59 to col. 12, line 32; buffer amount optimization of a controller changes/adjusts each buffer amount/capacity for class/QoS by updating buffer amount/capacity).

**Regarding Claims 33 and 43,** Hamada discloses a buffer element (see FIG. 1-2; ATM multiplexing apparatus; see col. 2, line 49-50; see col. 6, line 45-55) for a communication network (see FIG. 1, ATM network; see col. 1, line 20-25), the buffer element comprising:

- a first buffer memory (see FIG. 2, Highest priority FIFO buffer Q0) having a first capacity (see col. 6, line 65 to col. 7 line 4; see col. 11, line 60-67; cell count/capacity in a buffer, or buffer amount/capacity (i.e. Q0 buffer)) to store communication units (see col. 6, line 55-60; storing ATM cells) corresponding to a first quality of service level (see FIG. 2, storing in priority P0 class of highest QoS; see col. 6, line 56-63; col. 11, line 59-62);
- a second buffer memory (see FIG. 2, lower priority FIFO buffer Q1 or Q2) having a second capacity (see col. 6, line 65 to col. 7 line 4; see col. 11, line 60-67; cell count/capacity in buffer, or buffer amount/capacity (i.e. Q1 or Q2 buffer)) to store communication units (see col. 6, line 55-60; storing ATM cells) corresponding to a second quality of service level (see FIG. 2, storing in priority P1 or P2 class of lower QoS; see col. 6, line 56-63; col. 11, line 59-62); and

a buffer manager (see FIG. 1, a controller 14; see col. 6, line 45-50), coupled to the first buffer memory and the second buffer memory (see FIG. 1, controller 12 couples to Mux 12, which contains Q0 and Q1/2 buffers), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication units (see FIG. 2 and FIG. 3, step 1002,1004 with call admitted; see col. 6, line 52-64; see col. 11, line 55-57; QoS of each admitted cell is determined and stores in corresponding Q0, Q1 or Q2 buffer, respectively), to retrieve communication units from the first buffer memory and the second buffer memory (see FIG. 2; see col. 6, line 52-64; each buffered cell are outputted from Q0, Q1 or Q2 buffer, respectively), and to adjust at least one of the first capacity of the first buffer memory or the second capacity of the second buffer memory (see FIG. 4, step 1102,1104,1106,1108,1110,1112; see col. 11, line 59 to col. 12, line 32; buffer amount optimization of a controller changes/adjusts each buffer amount/capacity for class/QoS by updating buffer amount/capacity), based on a total memory available to the buffer element (see FIG. 3, step 1004; changing/updating according to total available bandwidth; see FIG. 4, total buffer amount L; see col. 11, line 50-56, 59-61), the first and second capacities (see FIG. 4, step 11-2; changing/updating according to buffer amount for class M (i.e. Q0) and class m (i.e. Q1 or Q2); see col. 12, line 7-11), and the quality of service provided by each buffer memory (see col. 11, line 59-65; changing/updating according to QoS of each priority classes buffer).

**Regarding Claims 8 and 42,** Hamada discloses wherein the communication units are ATM cells (see col. 6, line 55-60; storing ATM cells).

***Response to Arguments***

9. Applicant's arguments filed 7-14-2006 have been fully considered but they are not persuasive.

**Regarding claims 1,4,6,9,14,33,38,39,40 and 43, the applicant noted that,**  
“...amendments to the claims have been made solely for purpose of consistency...” in page 9, paragraph 1.

**In response to applicant's remark,** examiner agrees with the applicant since the amendment to the claims are replacing the word “**depth**” with “**capacity**”. As one skilled in the ordinary would clearly see that the word “**capacity**”, “**size**”, “**volume**”, or “**threshold**” of a buffer is essentially the same as “**depth**” of a buffer. Therefore, it is clear the claim language is consistent before and after amendment. Consequently, the rejections as set forth in previous office action are maintained.

**Regarding claims 1,2,4-9,11-17, the applicant argued that,** “...Fan fails to disclose...”a buffer manager...to adjust at least one of the first depth of first buffer memory or the second depth of the second buffer memory...” in page 8, paragraph 6; page 9, paragraph 2.

**In response to applicant's argument,** the examiner respectfully disagrees with the argument.

Fan discloses a **buffer element** (e.g., 30 or 31, Fig. 3) comprising a **first buffer** (e.g. CBR buffer/queue in 30 or 32, OPI or OLI, Fig. 3, and respective disclosure, col. 5, lines 25-28: col. lines 57-67), a **second buffer for a second QOS** (e.g., VBR, ABR or UBR buffer/queue in 30 or 32, OPI or OLI, Fig. 3, and respective disclosure), a **buffer manager** (e.g., the scheduler, inherent microprocessor/micro controller running the switch, or core, 34, Fig. 3 which stores

ATM cells in input buffers based on QoS, retrieves them, stores them in the output buffers, and retrieves them for outputting, col. 5, lines 55-59; col. 6, lines 13-21 and 43-56), a sorter (the controller which reads the ATM VPI/VCI header and decides which buffer to store the cells and/or the intermediate controllers such as the core, and the schedulers which control which output buffers the cells get stored in), buffers have depths/thresholds/capacities (**reads on buffer/queue capacity**) and **the depths/capacities get adjusted** (there is dynamic rate control and feedback which determines the current characteristics of the switch, the load or current capacity of the buffers and provides feedback to essentially load balance and control of buffer capacity; see dynamic rate based queues scheduler, Fig. 3 and respective, cols. 1-26, especially cols.7, line 45-col. 8, line 67; 44-55; col.9, lines 23-37; col. 10, lines 11-58; col. 12, line 4-col.1.line 34).

Moreover, Fan clearly discloses as follows:

**The basic principle is that each class queue is treated like a virtual source whose service rate is dynamically adjusted to reflect the unused bandwidth available at a bottleneck point in the switch.** Specifically, each class is serviced at its guaranteed minimum rate plus a dynamically adjusted fair share of any available unused bandwidth. Scheduling consists of computing the queue service rate and implementing the rate shaping function for all queues. An important feature of this approach to scheduling is that all queues are reduced to a generic set of queues, and the QoS perceived by the class is determined by the bandwidth guaranteed for the class. The generic queues are assigned to classes by the CAC. (see col. 10, line 11-25). (Emphasis added)

**Thus, it is clear that each class queue's length/source/capacity/size/threshold corresponds to a rate, which is dynamically adjusted.**

Fan discloses as follows:

**The closed-loop controller adjusts the rate  $E(n)$  such that the error  $\epsilon(n) = Q(n) - Q_{sub.0}$  decreases in absolute value. However, the dynamics of the aggregate input traffic  $R(n)$  may be faster than that of the closed-loop controller. The queue length,  $Q(n)$ , in the second stage may grow to a large value before the closed-loop**

controller can bring it close to the target value  $Q_{.sub.0}$ . This is caused by connections which transmit at rates significantly larger than their minimum guaranteed rates  $M_{.sub.i}$ . A large value of  $Q(n)$  can adversely affect the delay performance of connections which are transmitting at rates close to their minimum rates. Since the response time of the closed-loop controller may be too slow to prevent overload at the second stage of the scheduler, in the preferred embodiment a separate overload control mechanism is provided.

**When the second stage buffer exceeds a certain shape threshold, a feedback shape signal is transmitted to the DRC scheduler. This shape signal causes the scheduler to shape all queues at their guaranteed minimum rates,  $M_{.sub.i}$ , and stop distribution of unused bandwidth. This action provides a quick overload control mechanism allowing relief of congestion. See col. 12, line 29-55. (Emphasis added)**

**Thus, it is clear that each class queue's length/source/capacity/size/threshold with is associated rate is shaped/adjusted/controlled by DRC.**

Fan discloses as follows:

A closed-loop proportional-derivative controller is used to compute  $E$  based on observations of the aggregate virtual queue length at the OP bottleneck. When the OP channel utilization exceeds a value  $U_{.sub.0}$  (.apprxeq.95%, see step S110), **the controller adjusts the value of  $E$  so as to maintain the aggregate virtual queue length corresponding to the OP bottleneck close to a target value  $N_{.sub.0}$ .** When the OP channel utilization lies below  $U_{.sub.0}$ , the controller adjusts  $E$  so that utilization will be brought close to  $U_{.sub.2}$ . see col. 20, line 67 to col. 21, line 7. (Emphasis added)

**Thus, it is clear the queue length is adjusted according to the utilization.**

**Regarding claims 1,2,4-9,11-17, the applicant argued that, “...Fan does not disclose adjusting the depth or capacity of a buffer. In fact, as discussed in the Examiner interview, the capacity of the buffers in Fan remains fixed...Applicant have amended the claims to more clearly point out this feature...” in page 9, paragraph 1-2.**

**In response to applicant's argument, the examiner respectfully disagrees with the argument. Fan discloses adjusting the depth or capacity of a buffer as set forth in above response. During the interview, the examiner clearly explains his assertion of the how applicant broad limitation of “**buffer depth**” reads on Fan's “**class queue****

**length/source/capacity/size/****threshold**”. Consequently, examiner suggests to the applicant to revise claim in light of the specification in order to overcome the rejection set forth in the previous office. However, applicant fails to amend the claims to more clearly point out his invention since the amendment to the claims are simply replacing the word “**depth**” with the same meaning “**capacity**” (*also see above response*). Thus, the amendments made to claims do not overcome the prior arts set forth in previous rejection.

**Response to previous similar arguments with regards to Fan** as set forth in the previous office actions are hereby incorporated.

**Regarding claims 1,2,4-9,11-17,33-43, the applicant argued that**, “...Caldara fails to disclose...”a buffer manager...to adjust at least one of the first depth of first buffer memory or the second depth of the second buffer memory...” in page 9, paragraph 4; page 10, paragraph 2-5.

**In response to applicant's argument, the examiner respectfully disagrees with the argument.**

Caldara discloses a buffer manager (see **FIG. 1, a combined system of control in To/From Switch Port Processor 14/16 and Bandwidth Arbiter (BA) 12; see col. 4, line 32-64**), coupled to the first buffer memory and the second buffer memory (see **FIG. 1, a combined bandwidth control and Arbiter system couples to first and second priority queues/buffers**), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication units, and to retrieve communication units from the first buffer memory and the second buffer memory (see **FIG. 1, 6, a combined bandwidth and control system stores/writes/input and retrieves/read/output**

**the cells to/from first and second priority queues/buffers; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67), and to adjust a capacity of at least one of the first queue capacity of the first buffer memory or the second queue capacity of the second buffer memory (see col. 7, line 30-65; see col. 8, line 19 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined system of bandwidth control and arbiter dynamically manages/adjusts each queue for dynamic threshold/capacity).**

Moreover, Caldara discloses as follows:

By implementing this overall "list of lists" structure in the presently disclosed ATM switch, multiple levels of control are provided. For instance, the first time an event occurs which enables one cell to be transmitted to Port 0.sub.3, a cell from the first cell in the first queue associated with scheduling list 12 will be selected. This is cell C1 of Queue 3. **The pointers of the "Dynamic Bandwidth Lists" list and SLISTS 12 and 5 are adjusted such that SLIST 2 is the next scheduling list from which a cell is provided if dynamic bandwidth becomes available for transmission of a cell to output Port 0.sub.3. SLIST 5 would be second, and SLIST 12 would then be last.** Similarly, Queue 3, having just provided a cell, becomes the last queue to be eligible to provide a cell via a via SLIST 12, with Queue 11 being the next. This occurs through the manipulation of pointers in SLIST 12 and Queues 3 and 11. Finally, cell C1, having been transmitted, is dequeued from Queue 3, meaning the pointers of Queue 3 are readjusted to point to C2 as next to be transmitted. Only if another cell is received into Queue 3 will another cell fall in line behind cell 4. (see col. 8, line 19-37).

**Each queue for each connection has a dynamic bandwidth threshold 37 associated therewith, as shown in FIG. 4. If a queue buffer depth exceeds the cell depth indicated by the respective dynamic bandwidth threshold 37, the scheduling list for that queue will be added to the appropriate dynamic bandwidth list corresponding to the appropriate output port and priority. For each output port, the dynamic bandwidth list provides an indication of which if any cells are to be transmitted to the respective output port using dynamic bandwidth. The dynamic bandwidth threshold is established at call setup time. In a further embodiment of the present switch, however, the threshold value is adjusted dynamically based upon an empirical analysis of traffic through the switch.**

With regard to FIG. 7, a dynamic bandwidth threshold for a queue of CBR cells, or cells requiring a dedicated bandwidth, would be established such that the requested bandwidth (labelled "A" in FIG. 7) meets or exceeds the requirement. For other applications which may be more bursty but which still require tightly bounded delay, a **dynamic bandwidth threshold such as that labelled "B" in FIG. 7 may be suitable, wherein the majority of the traffic is handled by allocated bandwidth, with momentary bursts handled by high-priority dynamic bandwidth.** In either case, bandwidth specifically allocated but unused is made available to the BA by the TSPP for dynamic bandwidth allocation.

Note that for categories of service which rely solely on allocated bandwidth, **the dynamic bandwidth threshold is set above any expected peaks in cell reception**. Conversely, for categories of service having no (or low) delay bounds and no guaranteed bandwidth, such as UBR, **the dynamic bandwidth threshold is set to zero**. (see col. 9, line 6-40) (Emphasis added)

**In view of above, it is clear that “dynamic bandwidth threshold” value for each priority queue is dynamically adjusted.**

Regarding claims 1,2,4-9,11-17,33-43, the applicant argued that, “...Caldara does not disclose adjusting the depth or capacity of a buffer. In fact, as discussed in the Examiner interview, the capacity of the buffers in Caldara remains fixed...Applicant have amended the claims to more clearly point out this feature...” in page 9, paragraph 4; page 10, paragraph 2-5.

**In response to applicant's argument, the examiner respectfully disagrees** with the argument. Caldara discloses adjusting the depth or capacity of a buffer as set forth in above response. During the interview, the examiner clearly explains his assertion of the how applicant broad limitation of “**buffer depth**” reads on Cladara’s “**priority queue/buffer capacity/**  
**threshold**”. Consequently, examiner suggests to the applicant to revise claim in light of the specification in order to overcome the rejection set forth in the previous office. However, applicant fails to amend the claims to more clearly point out his invention since the amendment to the claims are simply replacing the word “**depth**” with the same meaning “**capacity**” (*also see above response*). Thus, the amendments made to claims do not overcome the prior arts set forth in previous rejection.

***Conclusion***

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on 571-272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*INM*

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8/2/06

*Doris H. To*

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